Amendments to the Claims:

1-15. (Cancelled)

16. (Currently Amended) A semiconductor package, comprising:

a leadframe having:

a chip paddle defining opposed top and bottom surfaces and a plurality of sides and corners; and

~~a plurality~~ **at least two sets** of leads extending along ~~at least one~~ **respective ones** of the sides of the chip paddle in spaced relation thereto, **each set of leads including at least two outer leads and at least one inner lead disposed between the outer leads, the inner and outer leads of each set** each ~~of the leads~~ defining opposed top and bottom surfaces, **with** the bottom surfaces of the **outer** leads **of each set each** being of ~~at least two difference lengths~~ **a first length and the bottom surface of the inner lead of each set being of a second length which is unequal to the first length**;

a semiconductor chip mounted to the top surface of the chip paddle and electrically connected to at least one of the **inner and outer** leads; and

an encapsulation material covering the leadframe and the semiconductor chip such that the bottom surfaces of the **inner and outer** leads~~, which are of at least two different lengths,~~ are exposed in the encapsulation material.

17. (Currently Amended) The semiconductor package of Claim 16 ~~wherein the leads are segregated into~~ **comprising** multiple sets **of leads** which extend ~~long~~ **along** respective ones of **each of** the sides of the chip paddle in spaced relation thereto.

18. (Cancelled)

19. (Currently Amended) The semiconductor package of Claim ~~18~~ **16** wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

20. (Currently Amended) The semiconductor package of Claim ~~18~~ **16** wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.

21. (Previously Presented) The semiconductor package of Claim 16 wherein the bottom surface of the chip paddle is exposed in the encapsulation material.

22. (Currently Amended) The semiconductor package of Claim 21 wherein:

the encapsulation material defines a generally planar bottom surface;

the bottom surface of the chip paddle is generally planar and substantially flush with the bottom surface of the encapsulation material; and

the bottom surfaces of the **inner and outer** leads are each generally planar and substantially flush with the bottom surface of the encapsulation material.

23. (Previously Presented) The semiconductor package of Claim 16 wherein the leadframe further comprises at least one tie bar attached to and extending from at least one of the corners of the chip paddle, the tie bar defining opposed top and bottom surfaces.

24. (Previously Presented) The semiconductor package of Claim 23 wherein the bottom surface of the at least one tie bar is exposed in the encapsulation material.

25. (Currently Amended) A semiconductor package comprising:

~~a plurality of leads, each of the leads defining opposed top and bottom surfaces, the bottom surfaces of the leads being of at least two different lengths;~~

a semiconductor chip defining multiple sides ~~and electrically connected to at least one of the leads~~; ~~and~~

at least two sets of leads extending along respective ones of the sides of the semiconductor chip in spaced relation thereto, each set of leads including at least two outer leads and at least one inner lead disposed between the outer leads, the inner and outer leads of each set each defining opposed top and bottom surfaces, with the bottom surfaces of the outer leads of each set each being of a first length and the bottom surface of the inner lead of each set being of a second length which is unequal to the first length, the semiconductor chip being electrically connected to at least one of the inner and outer leads; and

an encapsulation material covering the **inner lead, the outer** leads and the semiconductor chip such that the bottom surfaces of the **inner and outer** leads~~, which are of at least two different lengths,~~ are exposed in the encapsulation material.

26. (Currently Amended) The semiconductor package of Claim 25 ~~wherein the leads are segregated into~~ **comprising** multiple sets **of leads** which extend along respective ones of **each of** the sides of the semiconductor chip.

27. (Cancelled)

28. (Currently Amended) The semiconductor package of Claim ~~27~~ **25** wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

29. (Currently Amended) The semiconductor package of Claim ~~27~~ **25** wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.

30. (Currently Amended) The semiconductor package of Claim 25 wherein:

the encapsulation material defines a generally planar bottom surface; and

the bottom surfaces of the **inner and outer** leads are each generally planar and substantially flush with the bottom surface of the encapsulation material.

31. (Currently Amended) In a semiconductor package comprising a plurality of leads which each have a bottom surface which is exposed in an encapsulation material, and a semiconductor chip which **defines multiple sides,** is covered by the encapsulation material and electrically connected to at least one of the leads, the improvement comprising:

~~configuring the leads such that~~ **providing at least two sets of** the leads **which are extended along respective ones of the sides of the semiconductor chip and each** include at least two outer leads and at least one inner lead disposed between the outer leads, **with** the bottom surface of each of the outer leads **of each set** which is exposed in the encapsulation material ~~is~~ **being** of a first length, and the bottom surface of the inner lead **of each set** which is exposed in the encapsulation material ~~is~~ **being** of a second length which is unequal to the first length.

32. (Currently Amended) The semiconductor package of Claim 31 wherein **multiple sets of** the ~~semiconductor chip defines multiple sides, and the~~ leads are ~~segregated into multiple sets which each include at least two outer leads and at least one inner lead disposed between the outer leads, the leads of each set extending~~ **extended** along respective ones of **each of** the sides of the semiconductor chip.

33. (Cancelled)

34. (Previously Presented) The semiconductor package of Claim 31 wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

35. (Previously Presented) The semiconductor package of Claim 31 wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.